Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended)

An integrated circuit testing apparatus, comprising:

a ~~first~~ test circuit operable to produce a ~~first~~ signal for determining at least one of an operating reference signal and a substrate coupling effect on a plurality of components within an integrated circuit, said test circuit having a ring oscillator which mimics a data path within said integrated circuit, wherein said ring oscillator is powered by an external power supply; and

a ~~second~~ test circuit operable to produce a ~~second~~ signal for determining at least one of a cross-talk effect on said plurality of components and the accuracy of an interconnect capacitance extraction value.

Claim 2 (currently amended)

An integrated circuit testing apparatus, comprising:

a ~~first~~ test circuit operable to produce a ~~first~~ signal for determining at least one of an operating reference signal and a substrate coupling effect on a plurality of components within an integrated circuit, said test circuit having a ring oscillator which mimics a data path within said integrated circuit, wherein said ring oscillator is powered by an external power supply; and

a ~~third~~ test circuit operable to produce a ~~third~~ signal for determining at least one of an effect of system noise on the operational speed of said plurality of components and a maximum degradation expected for a logic path between said plurality of components.

Claim 3 (currently amended)

An integrated circuit testing apparatus, comprising:

a ~~first~~ test circuit operable to produce a ~~first~~ signal for determining at least one of an operating reference signal and a substrate coupling effect on a plurality of components within an integrated circuit; and

a ~~fourth~~ test circuit operable to produce a ~~fourth~~ signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components.

Claim 4 (currently amended)

An integrated circuit testing apparatus, comprising:

a ~~second~~ test circuit operable to produce a ~~second~~ signal for determining at least one of a cross-talk effect on ~~said~~ a plurality of components within an integrated circuit and the accuracy of an interconnect capacitance extraction value, said test circuit having a ring oscillator routed within a core logic area of said integrated circuit, wherein said ring oscillator is powered by an external power supply; and

a ~~third~~ test circuit operable to produce a ~~third~~ signal for determining at least one of an effect of system noise on the operational speed of said plurality of components and a maximum degradation expected for a logic path between said plurality of components.

Claim 5 (currently amended)

An integrated circuit testing apparatus, comprising:

a ~~second~~ test circuit operable to produce a ~~second~~ signal for determining at least one of a cross-talk effect on ~~said~~ a plurality of components within an integrated circuit and the accuracy of an interconnect capacitance extraction value; and

a ~~fourth~~ test circuit operable to produce a ~~fourth~~ signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components.

Claim 6 (currently amended)

An integrated circuit testing apparatus, comprising:

a ~~third~~ test circuit operable to produce a ~~third~~ signal for determining at least one of an effect of system noise on the operational speed of ~~said~~ a plurality of components within an integrated circuit and a maximum degradation expected for a logic path between said plurality of components; and

a ~~fourth~~ test circuit operable to produce a ~~fourth~~ signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components.

Claim 7 (canceled)

Claim 8 (currently amended)

The apparatus of claims 1~~, 4,~~ or 5 wherein said ~~second~~ test circuit operable to produce a signal for determining at least one of a cross-talk effect on said plurality of components within said integrated circuit and the accuracy of an interconnect capacitance extraction value includes a ~~further comprises a second ring oscillator, said second~~ ring oscillator ~~being~~ routed within a core logic area of said integrated circuit ~~and being~~ ,wherein said ring oscillator is powered by an external power supply.

Claim 9 (currently amended)

The apparatus of claims 2 or 6 wherein said ~~third~~ test circuit operable to produce a signal for determining at least one of an effect of system noise on the operational speed of said plurality of components within said integrated circuit and a maximum degradation expected for a logic path between said plurality of components includes a ~~further comprises a third ring oscillator, said third~~ ring oscillator ~~being~~ randomly located within a core logic area of said integrated circuit ~~and being~~ , wherein said ring oscillator is powered by an external power supply.

Claim 10 (currently amended)

The apparatus of claims 3 or 6 wherein said ~~fourth~~ test circuit operable to produce a signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components within said integrated circuit includes a ~~further comprises a fourth ring oscillator, said fourth~~ ring oscillator ~~being routed to mimic~~ which mimics a data path within said integrated circuit ~~and sharing~~ , wherein said ring oscillator shares a power supply with a core logic area of said integrated circuit.

Amendments to the Drawings:

A new page, Figure 10, is added to the drawings to offer a more detailed illustration of the features of operation 903 as found in Figure 9. Support for new Figure 10 may be found in paragraphs 65 – 66. One (1) page of new formal drawings (i.e., Figure 10) is submitted herewith. No new matter is added.